Code No: 154AN **R18**

JAWAHARLAL NEHRU TECHNOLOGICAL UNIVERSITY HYDERABAD

B. Tech II Year II Semester Examinations, February - 2024

DIGITAL ELECTRONICS

(Electrical and Electronics Engineering)

Time: 3 Hours **Max. Marks: 75**

Note: i) Question paper consists of Part A, Part B.
ii) Part A is compulsory, which carries 25 marks. In Part A, answer all questions.
iii) In Part B, Answer any one question from each unit. Each question carries 10 marks and may have a, b as sub questions.

PART – A

(25 Marks)

1.a)	Define the terms Propagation delay and Power dissipation.	[2]
b)	What are the advantages of Schottky TTL family?	[3]
c)	What is priority encoder?	[2]
d)	Express Gray code 1011 into binary numbers.	[3]
e)	What is the difference between latch and flip flop?	[2]
f)	Draw the state table and excitation table of T flip flop.	[3]
g)	State the advantages and applications of sample and hold circuits.	[2]
h)	Find the resolution of a 12 bit DAC converter.	[3]
i)	Compare ROM and RAM.	[2]
j)	Distinguish between volatile and non-volatile memory.	[3]

PART – B

(50 Marks)

2. Obtain Minimal POS expression and realize using only NAND and NOR gates
$F = \sum m (0,2,3,6,7) + d(8,10,11,15)$. [10]

OR

3.a) Draw the circuits of 2-input NAND and 2 input NOR gate using CMOS.
b) Obtain 3 level NOR – NOR implementation of f = [ab + cd] ef. [6+4]

4.a) Design and explain the circuit of 4 to 1 Mux.
b) Implement full subtractor using Demultiplexer. [4+6]

OR

5. Draw and explain the block diagram of a 4-bit serial adder to add contents of two registers. [10]

6.a) Design and explain the BCD ripple counter with timing diagram.
b) Differentiate Asynchronous and Modulus counter. [8+2]

OR

7.a) Design and explain the working of an 4-bit Up/Down Parallel counter.
b) What is race around condition? How do you eliminate it? [8+2]

8.a) With neat diagram explain the flash type A/D converter.
b) With functional block diagram explain the voltage to time converter. [5+5]

OR

9.a) Explain the R-2R Ladder type D/A converter with suitable diagrams.
b) With neat diagram, discuss on the single slope ADC. [5+5]

10.a) Write difference between PLA and PAL.
b) Derive a combinational circuit defined by the function, F1 = AB'C'+AB'C+ABC and F2 = A'BC+AB'C+ABC using PLA with minimal AND gates. [4+6]

OR

11. Describe the classification of semiconductor memories in detail. [10]

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